REMARKS

In that Action dated August 28, 2003, having a shortened statutory period set to expire November 28, 2003, the Examiner has rejected claims 1 and 3, and dependent claims 4-6 under 35 U.S.C. § 112, *second paragraph*, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the Applicant regards as the invention. Specifically, the Examiner believes that in claims 1 and 3 the term "terminal bridge" is not defined in the specification in such a way as to give clear meaning to what is being claimed. Applicant respectfully disagrees with the Examiner's position for the following reasons.

As set forth in the present specification, page 13, lines 8 et seq. and as illustrated within Figure 3, multiple terminal bridges are described and depicted. Each terminal bridge is described in the specification as being configured to prevent the propagation of errors up into the PCI host bridge and into higher levels of the data processing. Further, Applicant respectfully urges the Examiner to consider Figure 7 in which a single terminal bridge 702 is illustrated and described in the present specification at page 23, lines 7 et seq. As set forth in the aforementioned portion of the specification, terminal bridge 702 includes an arbiter 714 which controls access to PCI bus 716. Bus request signals 710 from input/output adapters are fed into arbiter 714 which then determines which input/output adapter gets to utilize the bus and thereafter arbiter 714 signals that input/output adapter via a grant signal. The grant signals permit terminal bridge 702 to utilize the appropriate set of range registers 712 which are assigned to that particular input/output adapter.

Thus, a "terminal bridge" is described in the present specification, illustrated in great detail within Figure 7 and specified in terms of its functionality. Further, Applicant submits

herewith for the use of the Examiner, page 686 of the IBM Dictionary of Computing, 10th Edition, August 1993, in which the word "terminal" is defined as "a functional unit in a system or communication network at which data may enter or leave." Applicant also submits page 73 of the aforementioned IBM Dictionary of Computing in which the term "bridge" is defined as "a functional unit that interconnects two local area networks that use the same logical control protocol but may use different medium access protocols" or "in the connection of local loops, channels, or rings, the equipments and techniques utilized to match circuits and to facilitate accurate data transmission."

Thus, Applicant urges the Examiner to consider that terminal bridge 702, as illustrated and described with respect to Figure 7 of the present application, is interposed between PCI host bridge 704 and I/O adapters 700 and receives data on the buses therebetween. Thus, an entity which receives data and is interposed between two other devices can have no clearer description than "terminal bridge" as that term is utilized in the present specification and the Examiner's objection of that term in not believed to be well founded.

In view of the above, the Applicant urges the Examiner to withdraw the rejection of these claims under 35 U.S.C. § 112, *second paragraph*.

Next, the Examiner has rejected claims 1-6 under 35 U.S.C. § 103(a) as being unpatentable over United States Patent No. 4,843,541, issued to *Bean et al.*, in view of United States Patent No. 6, 438,671, issued to *Doing et al.* That rejection is respectfully traversed.

As set forth in claim 1, for example, the logically partitioned data processing system of the present invention is described as a plurality of input/output adapters each one of which is associated with a different one of the plurality of logical partitions which are described. These

multiple input/output adapters are connected to a terminal bridge which is interposed between those input/output adapters and the data transmission bus, and which prevents transmission of data between a given one of the multiple input/output adapters and the data transmission bus.

In contrast, *Bean et al.* describes a partitioned data processing system which utilizes multiple Virtual Machines (VM). As set forth within *Bean et al.* at column 1, lines 35 et seq., in a Virtual Machine (VM) system, each user is given "an apparent or logical CPU." and "Plural Logical CPUs could share each real CPU resource(s) in the system." (*emphasis added*). Thus, unlike the claims of the present application, in a Virtual Machine (VM) system all actual resources within the system are accessible by each Virtual Machine (VM). The mere utilization of address translation so that portions of the system memory are assigned to a particular Virtual Machine (VM), does not, in the opinion of the Applicant, show or suggest in any way the physical limitation of a plurality of input/output adapters in a manner which is set forth expressly within the claims of the present application, and *Bean et al.* is believed not to be a valid reference for rejecting the claims of the present application, in that *Bean et al.* fails to show or suggest in any way the physical limitation of access to one of a plurality of input/output adapters utilizing a terminal bridge, as described within the present specification.

The Examiner cites *Doing et al.*, in view of *Bean et al.*'s failure to explicitly teach a data transmission bus and a terminal bridge connected to that data transmission bus, noting that the use of buses and bus bridges is well known in the computer art. The Examiner cites *Doing et al.* and notes that Figure 1 thereof teaches multiple input/output processing units. *Doing et al.* indeed teaches the use of multiple input/output processing units; however, nothing within *Doing et al.* shows or suggests the interposition of a terminal bridge between each of those multiple input/output processing devices and bus interface 105, as expressly set forth within the claims of

the present application. Consequently, Applicant urges that *Doing et al.* cannot be said to show or suggest the invention set forth within the present claims.

In summary, *Bean et al.* teaches a Virtual Machine (VM) in which each logical CPU has access to all resources of the system and *Doing et al.* teaches a system having multiple input/output processing units. Nothing within either reference, whether considered alone or in combination, shows or suggests the invention set forth within the present claims wherein multiple input/output adapters are provided and data transmission between each individual input/output adapter is limited utilizing a terminal bridge as described in the present specification and as set forth within these claims. Consequently, Applicant urges that the Examiner's rejection of claims 1-6 over this combination of references is not well founded and it should be withdrawn.

The Examiner has also rejected claims 3, 5 and 6 under 35 U.S.C. § 103(a) as being unpatentable over *Bean et al* and. *Doing et al.* and further in view of Applicant's prior art. The Examiner notes that Applicant admits that DMA address range registers are known in the prior art and are typically utilized to restrict ranges within main storage memory. However, nothing within Applicant's admitted prior art shows or suggests in any way the utilization of address range registers interposed between an input/output adapter and a data transmission line in the manner set forth within the present claims and Applicant urges that the only suggestion for such combination comes from the present specification. Consequently, one having ordinary skill in the art would find no suggestion within the prior art for a combination of DMA address range registers with a method and system for controlling input/output adapters as set forth within the present claims and the Examiner's rejection of claims 3, 5 and 6 is also not believed to be well founded.

The Examiner has also rejected claim 4 under 35 U.S.C. § 103(a) as being unpatentable over *Bean et al.* and *Doing et al.* and the admitted prior art, and further in view of United States Patent No. 6,584,530, issued to *Kondo et al.* That rejection is not well founded and it should be reversed.

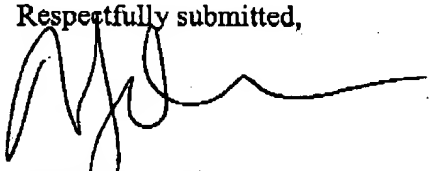
Kondo et al. teaches the utilization of a bus converter 1 within Figure 1 which, through input/output bus 18, is coupled to multiple input/output devices. The bus arbiter described therein is utilized to prevent low-speed input/output accesses from obstructing transactions with main storage and does not, in any way, shape or form, prevent transmission of data to locations which are unassigned in logical partitions to a particular input/output device as expressly set forth within the claims of the present application. Consequently, Applicant urges that this rejection is not well founded and it should be withdrawn.

The Examiner has also issued a rejection under the judicially created doctrine of double patenting of co-pending application 09/589,665. The Examiner notes that "this application fails to claim a data transmission bus and a terminal bridge connected to that data transmission bus, but goes on to note that these elements are well known in computer systems." Applicant urges the Examiner to consider that having initially rejected Applicant's claims for failure to define the term "terminal bridge" the Examiner's position asserting that a "terminal bridge" is "well known in computer systems." is not logically defensible. In view of the distinct differences between claim 1 of the present application and claim 1 of the co-pending application, Applicant traverses the obviousness-type double patenting rejection, but reserves the right to submit a terminal disclaimer at sometime in the future.

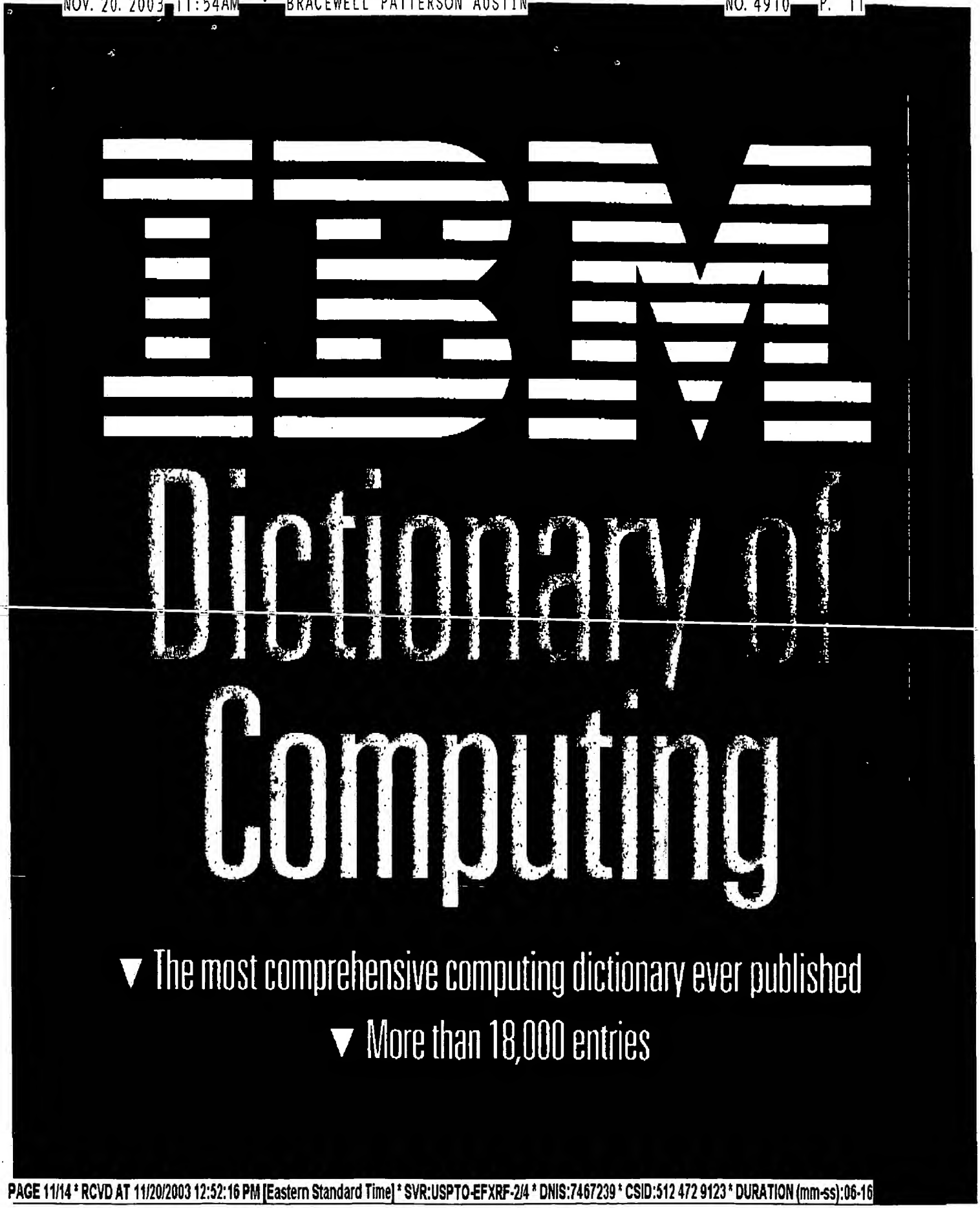
For the reasons set forth herein, Applicant urges that claims 1-6 define patentable subject matter over the cited prior art and withdrawal of all rejections and passage of this application to issue is therefore respectfully requested.

No extension of time is believed to be necessary. However, in the event an extension of time is required, that extension of time is hereby requested. Please charge any fee associated with an extension of time to IBM Corporation Deposit Account No. 09-0447.

Respectfully submitted,



Andrew J. Dillon
Reg. No.29,634
BRACEWELL & PATTERSON, L.L.P.
P.O. Box 969
Austin, Texas 78767-0969
(512) 542-2100
ATTORNEY FOR APPLICANTS



Limitation of Liability

While the Editor and Publisher of this book have made reasonable efforts to ensure the accuracy and timeliness of the information contained herein, neither the Editor nor the Publisher shall have any liability with respect to loss or damage caused or alleged to be caused by reliance on any information contained herein.

5 6 7 8 9 0 DOC/DOC 9 9 8 7

ISBN 0-07-031488-8 (HC)
ISBN 0-07-031489-6 (PBK)

The sponsoring editor for this book was Daniel A. Gonneau and the production supervisor was Thomas G. Kowalczyk.

Printed and bound by R. R. Donnelley & Sons Company.

Tenth Edition (August 1993)

This is a major revision of the *IBM Dictionary of Computing*, SC20-1699-8, which is made obsolete by this edition. Changes are made periodically to the information provided herein.

It is possible that this material may contain reference to, or information about, IBM products (machines and programs), programming, or services that are not announced in your country. Such references or information must not be construed to mean that IBM intends to announce such IBM products, programming, or services in your country. Comments may be addressed to IBM Corporation, Department E37/656, P. O. Box 12195, Research Triangle Park, NC 27709.

International Edition

Copyright © 1994 by International Business Machines Corporation. Exclusive rights by McGraw-Hill, Inc. for manufacture and export. This book cannot be re-exported from the country to which it is consigned by McGraw-Hill. The International Edition is not available in North America.

When ordering this title, use ISBN 0-07-113383-6.

This book is printed on acid-free paper.

external intervention, are convenient for resuming execution. (T) (2) An instruction in a program for halting execution. Breakpoints are usually established at positions in a program where halts, caused by external intervention, are convenient for restarting. (T) (3) A place in a program, specified by a command or a condition, where the system halts execution and gives control to the workstation user or to a specified program. (4) See instruction address stop. Synonymous with breakpoint instruction, dynamic stop.

breakpoint halt A closed loop consisting of a single jump instruction that effects a jump to itself; it is often used to achieve a breakpoint. (I) (A) Synonymous with breakpoint instruction, dynamic stop.

breakpoint instruction Synonym for breakpoint halt.

breakpoint program In a batch job, a user program that can be invoked when a breakpoint is reached.

break sequence In start-stop protocol, the transmission of all 0 bits.

break signal A signal sent over a remote connection to interrupt current activity on the remote system.

break statement A C language control statement that contains the keyword "break" and a semicolon.

breakup In video presentations, disruptions in a signal caused by damage to the tape or disc or by loss of sync.

break value In AIX data segment space allocation, the address of the first location beyond the current end of the data segment.

B-register Deprecated term for index register.

bridge (1) A functional unit that interconnects two local area networks that use the same logical link control protocol but may use different medium access control protocols. (T) (2) A functional unit that interconnects multiple LANs (locally or remotely) that use the same logical link control protocol but that can use different medium access control protocols. A bridge forwards a frame to another bridge based on the medium access control (MAC) address. (3) In the connection of local loops, channels, or rings, the equipment and techniques used to match circuits and to facilitate accurate data transmission.

Note: A bridge connects networks or systems of the same or similar architectures, whereas a gateway connects networks or systems of different architectures.

bridge input circuit In process control, an analog input circuit in which the sensing component of the technical process is in one branch of the bridge and the reference components in another. (T)

Note: The reference bridge voltage is usually supplied by the user.

bridge tap An unterminated length of line attached somewhere between the extremities of a telecommunication line. Bridge taps are undesirable. Contrast with terminated line.

bridging In OCR, a combination of peaks and smudges that may close or partially close a loop of a character.

bring-up The process of starting a computer system or a subsystem that is to operate under control of the system.

bring-up test In the IBM 8100 Information System, test modules contained in read-only storage, that verify the capability of selected functions within the system.

broadband (1) A frequency band broad enough to be divided into several narrower bands, each of which can be used for different purposes or be made available to different users. Synonymous with wideband. (T) (2) A frequency band divisible into several narrower bands so that different kinds of transmissions such as voice, video, and data transmission can occur at the same time. Synonymous with wideband. See also baseband. (3) Transmission media and techniques that use a broad frequency range, divided into sub-bands of narrower frequency, so that different kinds of transmission can occur at the same time.

broadband channel A data transmission channel 6MHz wide. (T)

broadband exchange (BEX) A public switched telecommunication system of Western Union, featuring various bandwidth duplex connections.

broadband LAN A local area network in which data are encoded, multiplexed, and transmitted with modulation of carriers.

Note: A broadband LAN consists of more than one channel. (T)

broadband signaling In a network, transmission using analog signals, carrier frequencies, and multiplexing techniques to allow more than one node to transmit at a time. Contrast with baseband signaling.

Note: Multiple channels or frequency bands can be created by using frequency-division multiplexing (FDS).

temporary objects In the AS/400 system, objects, such as data paths or compiler work areas, that are automatically deleted by the system when the operating system is loaded.

temporary read/write error An error that is eliminated by retrying a read/write operation.

temporary storage In computer programming, storage locations reserved for intermediate results. (A) Synonymous with working storage.

temporary text delay (TTD) A control character sequence sent by a transmitting station either to indicate a delay in transmission or to initiate an abort of the transmission in progress.

temporary-text-delay (TTD) character In BSC, a transmission control character that is used to maintain the data link when no text is being transmitted. TTD indicates to the receiving station that there is a temporary delay in transmission of data.

tens complement The radix complement in the decimal numeration system. (I) (A) Synonymous with complement-on-ten.

tensile strength A measure of the tension that a material such as continuous forms can accept without tearing.

tensioning In the 3800 Printing Subsystem, stretching or causing extension of continuous forms while they are threaded in the printer.

tera (1) Ten to the twelfth power; 1,000,000,000,000 in decimal notation. When referring to storage capacity, two to the fortieth power; 1,099,511,627,776 in decimal notation. (2) A unit of measure equal to 10^{12} bytes; 1 000 000 000 000 in decimal notation.

term (1) A construct in a conceptual schema language that refers to an entity. (T) (2) The smallest part of an expression that can be assigned a value. (3) See absolute term, arithmetic term, logical term, relocatable term.

terminal (1) A functional unit in a system or communication network at which data may enter or leave. (T) (2) A point in a system or communication network at which data can either enter or leave. (A) (3) A device, usually equipped with a keyboard and display device, capable of sending and receiving information. (4) In COBOL, the originator of a transmission to a queue, or the receiver of a transmission from a queue.

Note: The terms terminal and workstation are often used interchangeably. However, a terminal may not have a human operator. A workstation is a terminal at which a human operator performs an application.

terminal access facility (TAF) In the NetView program, a facility that allows a network operator to control a number of subsystems. In a full-screen or operator control session, operators can control any combination of such subsystems simultaneously.

terminal address card In a 3600 Finance Communication System, an addressable logic element that connects a terminal to a local loop or to a subloop, and that handles signals passing through the terminal. Synonymous with terminal loop adapter.

terminal component A separately addressable part of a terminal that performs an input or output function, such as the display component of a keyboard-display device or a printer component of a keyboard-printer device.

terminal configuration facility (TCF) A set of macrostatements to be coded by the user and modules in programmable store system host support that are used to define and create the terminal operational environment.

terminal control address space (TCAS) The part of TSO/VTAM that provides logon services for TSO/VTAM users.

Terminal Control table (TCT) A table describing a configuration of terminals, logical units, or other CICS systems in a CICS network with which the CICS system communicates.

terminal descriptor In the AIX object data manager (ODM), a named variable of the type short, long, binary, char, or vchar used to define the basic data types in an ODM object class definition. See also binary, char, long, object class, short, vchar.

terminal display language (TDL) A set of SPPS II statements coded by the application programmer to control the IBM 3275 Display Station screen. These statements define the formats of data to be transferred between a keyboard/display and an application program buffer. They require translation by the terminal definition language translator. See also transformation definition language.

terminal emulation The capability of a microcomputer or personal computer to operate as if it were a particular type of terminal linked to a processing unit and to access data. See also download, upload.

terminal emulator A program that allows a device such as a microcomputer or personal computer to enter and receive data from a computer system as if it were